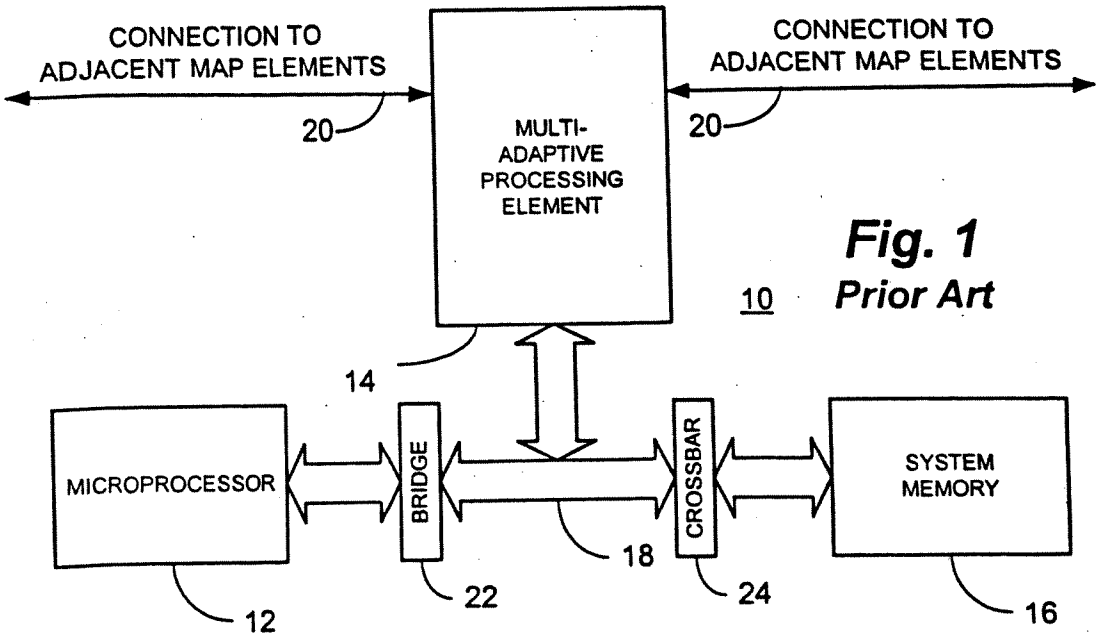


Fig. 1
10 *Prior Art*

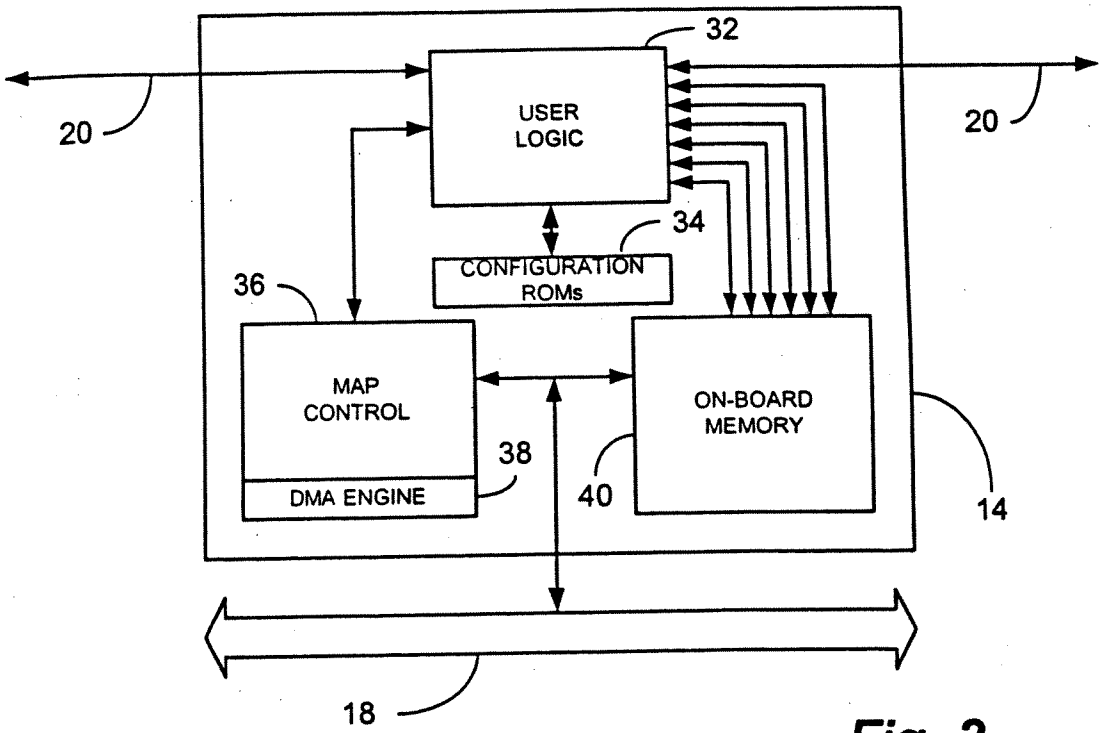


Fig. 2
Prior Art

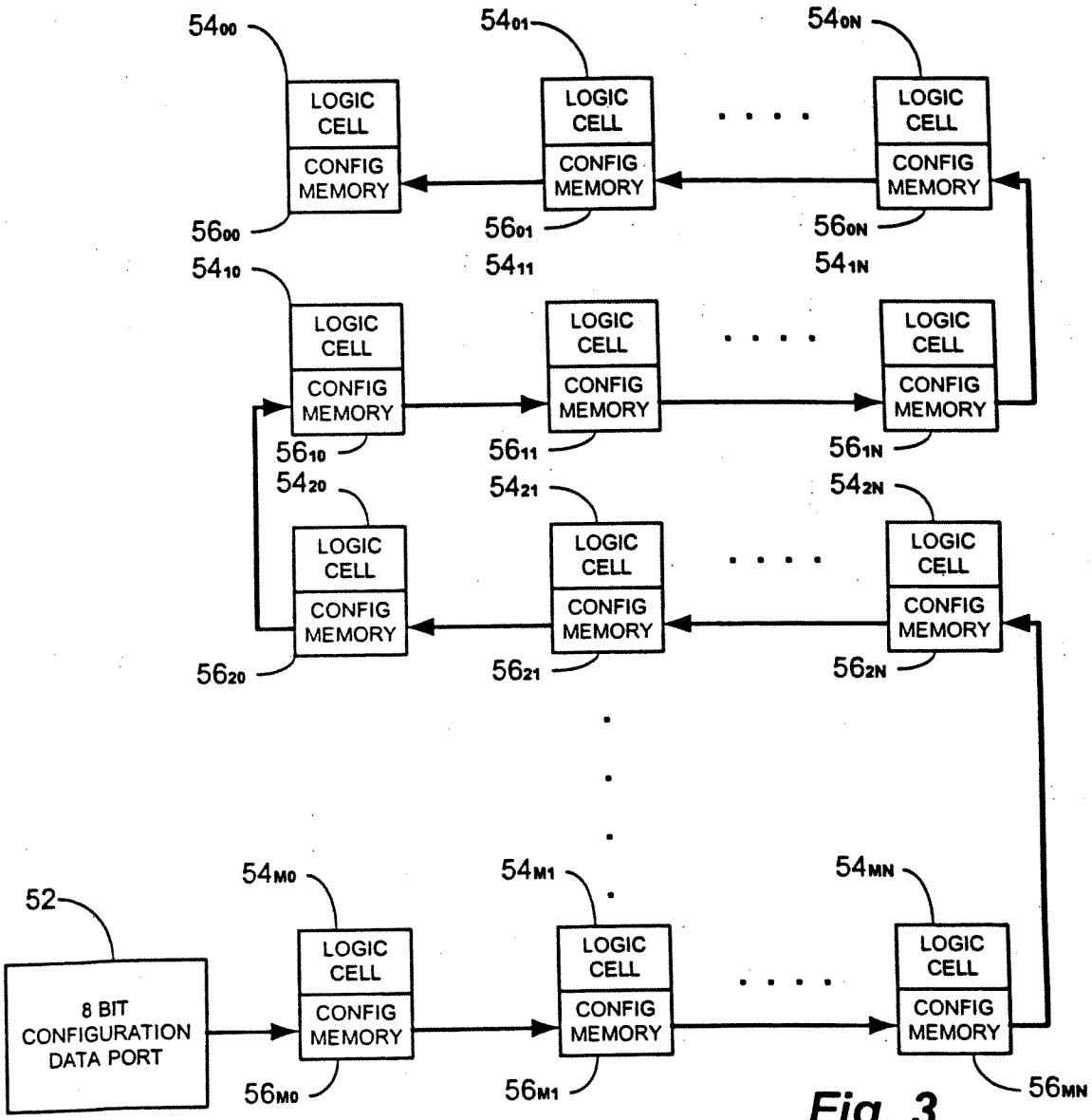


Fig. 3
Prior Art

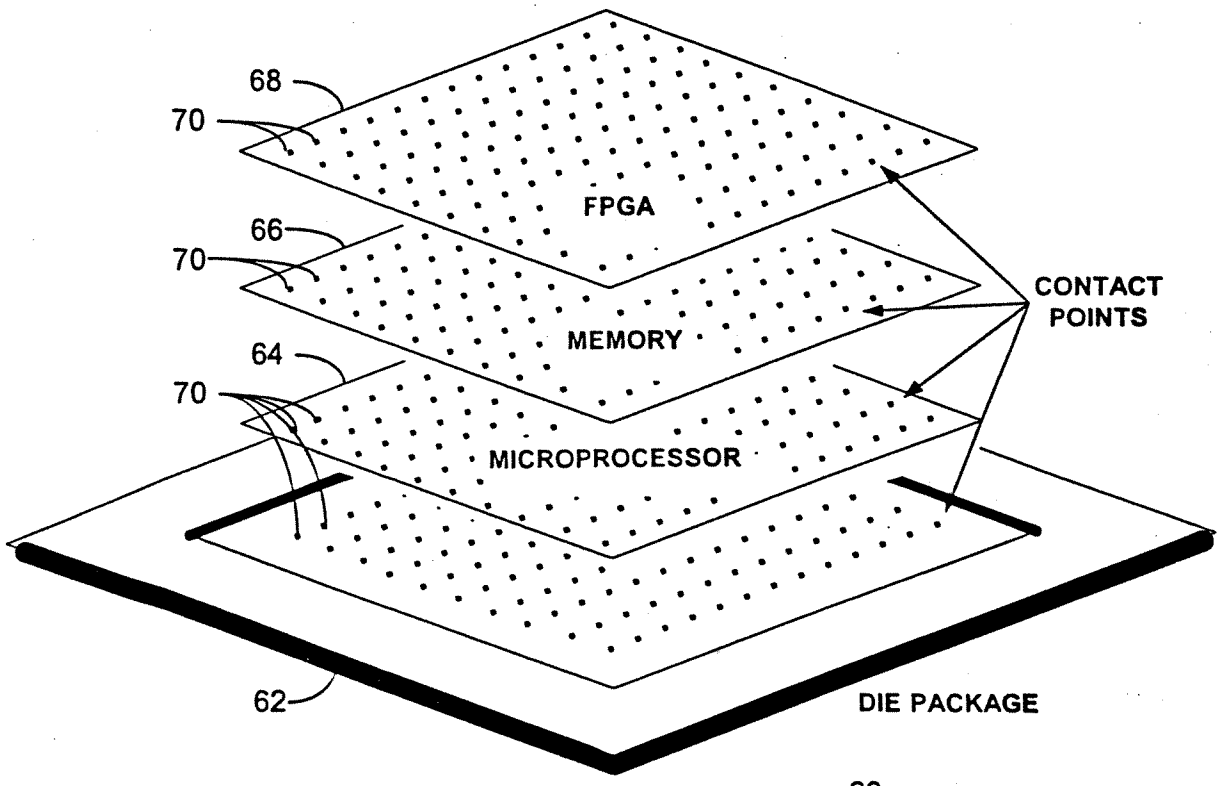
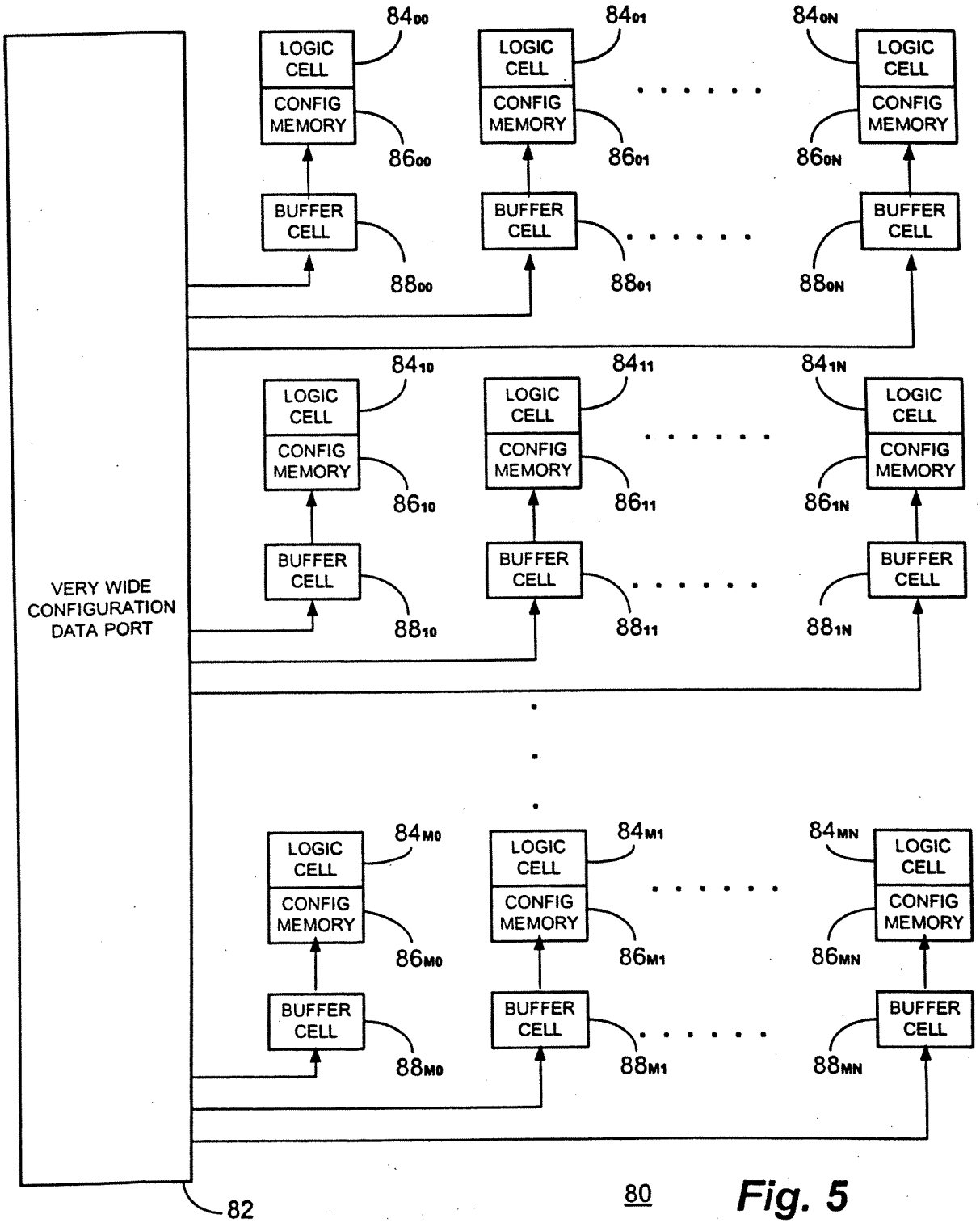

68
70
FPGA
66
70
MEMORY
64
70
MICROPROCESSOR
CONTACT POINTS
62
DIE PACKAGE
60

Fig. 4


VERY WIDE CONFIGURATION DATA PORT
82
LOGIC CELL
CONFIG MEMORY
BUFFER CELL
84_{00}
86_{00}
88_{00}
84_{01}
86_{01}
88_{01}
84_{0N}
86_{0N}
88_{0N}
84_{10}
86_{10}
88_{10}
84_{11}
86_{11}
88_{11}
84_{1N}
86_{1N}
88_{1N}
84_{M0}
86_{M0}
88_{M0}
84_{M1}
86_{M1}
88_{M1}
84_{MN}
86_{MN}
88_{MN}

80

Fig. 5

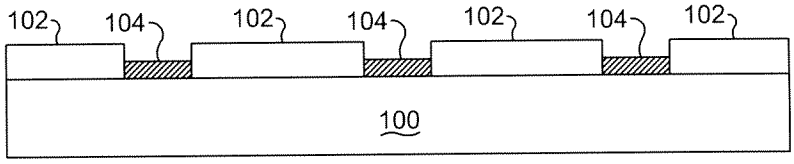


Fig. 6

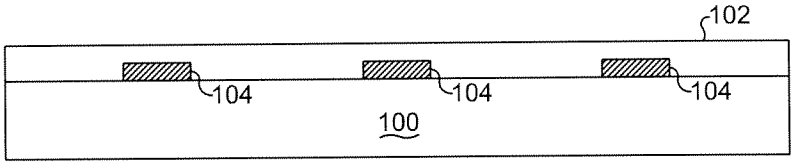


Fig. 7

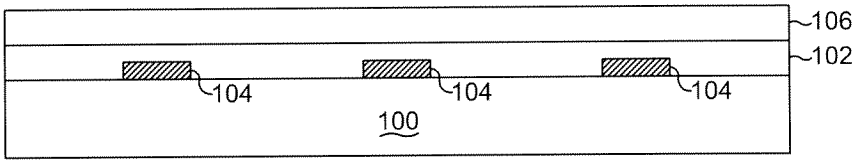


Fig. 8

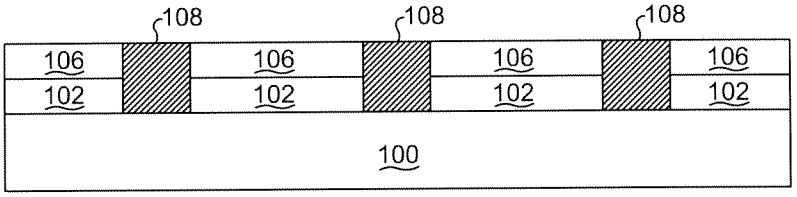


Fig. 9

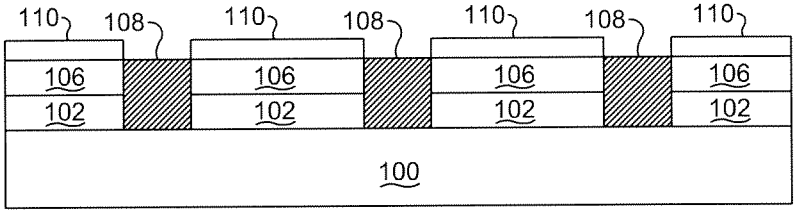


Fig. 10

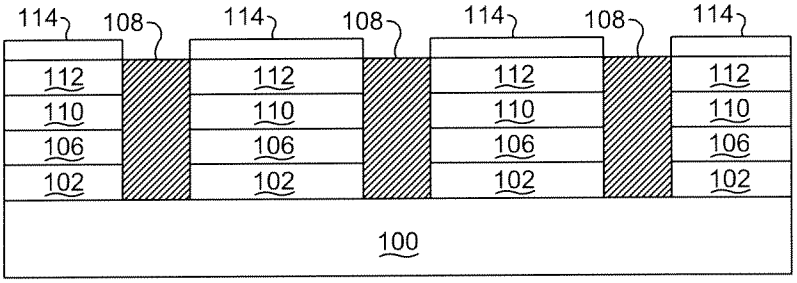


Fig. 11